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#PremiumTech

DEALING WITH SIC MOSFETS IN POWER DESIGN

SiC MOSFETs for State of the Art Design

DEALING WITH SIC MOSFETS IN POWER DESIGN

Miquel Gonzalez
Engineering Manager

At Premium we were pioneers 15 years ago when we first introduced SiC technology in our power solutions with the first generations of 1200V schottky diodes. Nowadays, the use of SiC diodes is part of a large number of our standard and customized solutions.

Once again, we include the use of SiC MOSFEF in our designs, providing great advantages in applications of over 600V. In comparison, SiC vs. Si MOSFETS offer:

- A drastic reduction in the specified ON-Resistance, especially for applications over 900V
- Less variation of ON-Resistance with temperature
- A large reduction in internal capacities

With these characteristics it is possible to achieve, compared with the use of 1200V IGBTs:

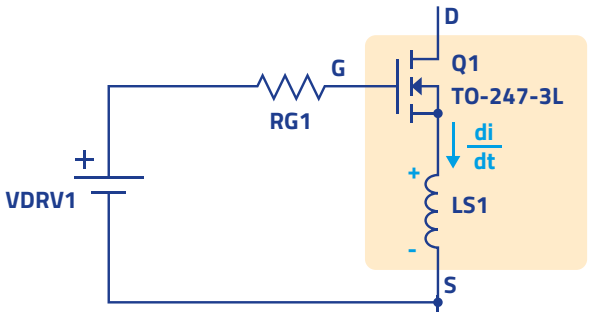
- Up to 30% lower losses
- 2-3 x faster switching speed
- 30% fewer components
- Lower overall system cost

On the other hand, the use of SiC MOSFETS requires an extra dose of RDI knowledge in order to overcome challenges that its use entails.

New encapsulations for SiC MOSFETs:

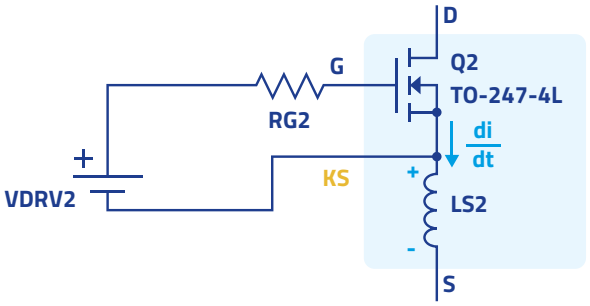
These devices can withstand high power densities thanks to their combination of low conduction and switching losses, high operating junction temperatures, and fast switching speeds.

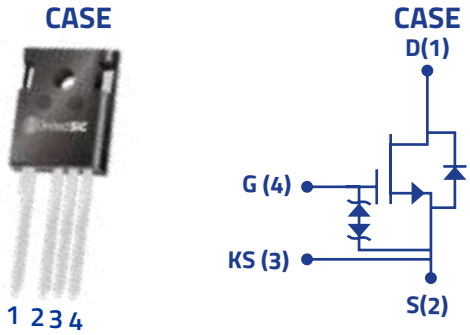
High power densities are attractive for smaller power control and conversion circuits but cannot be achieved solely by choosing a semiconductor material. It is necessary for these devices to be integrated in packages with low thermal resistance, such as TO-247. Unfortunately TO-247 package connections often have high inductances, which can limit switching speeds. When switching a MOSFET at high frequency, the connection from the source to the device is a common point for the gate driver voltage and the source drain current.



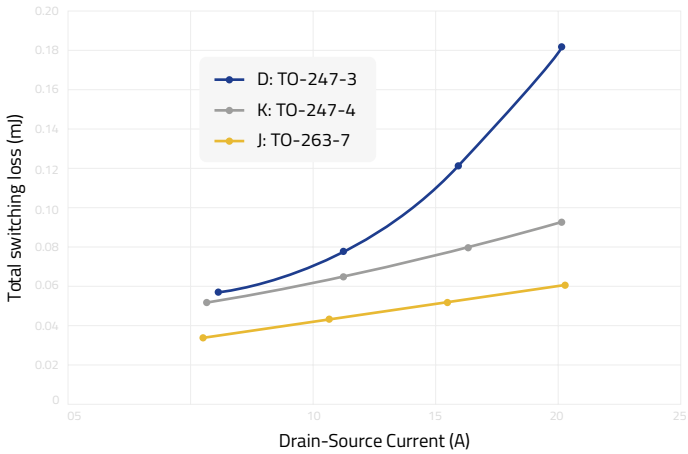
Due to the common LS1 inductance, changes in current will affect the gate voltage in proportion to the LS1 and the current change rate. When the gate is turned off, the voltage appearing on the inductance acts to maintain the gate voltage for a longer time, slowing down the current drop through the device. When the MOSFET turns on, the voltage induced in the L coil acts to slow down the rise in current. This effect is critical in SiC transistors, as they can switch tens of amps in just a few nanoseconds. This effect causes a switching loss increase.

To solve this effect, the manufacturers of these devices have developed new packages with a Kelvin connection to ensure that the return of the device's gate is as close as possible to the connection of the source in the MOSFET itself.





MOSFET manufacturers have added a fourth pin to the TO-247 package (when superior heat dissipation characteristics are required) and also to the SMD TO-263 package. This way the switching losses of the same device notably improves with the choice of encapsulation, as shown in the following figure:



Most critical PCB layout:

Due to these devices´ high switching speeds and high power density, the capacities and parasitic inductances of PCBs must be considered, as they become crucial in the design when efficiency is to be maximized.

To minimize the parasitic capacities and reduce the coupling, the tracks need to be as short and small as possible (example: for 1cm2 of trace overlap there is a parasitic capacity of 38pF that can increase the switching losses and generate EMI problems). And in order to minimize parasitic inductances it is also necessary to reduce the length of the tracks. This way, voltage spikes are reduced (example: for a 50mm long and 10mm wide track, the PCB´s inductance is 28.5nH, which with a typical di/dt for this technology can generate a voltage spike of 70V).

High dv/dt tracks are critical in PCB design:

- Sensitive signals should be kept away from these tracks
- Coupling and parasitic capacity of these tracks should be minimized to avoid EMI problems in the design of the final product
- Sensitive signals should be kept away from high magnetic field such as resonant choke and power transformer

The design of high di/dt loops is also critical:

- It is necessary to put ceramic capacitors or film caps as close as possible to minimize the high frequency di/dt loop
- The positioning on the PCB layout of the power components needs to be taken into consideration in order to minimize the high frequency di/dt loop

Overall, it is necessary to use PCB structures with at least 4 layers with the following distribution:

Superimposing sensitive signal and power tracks should be avoided and a 3rd track of GND is used to act as shielding to cover the signal tracks and the device driver.

Driver design and its most critical feeding:

Due to high switching speeds of these devices, it is necessary to use newer driver generations, capable of facing the challenge posed by these transistors. These drivers must have:

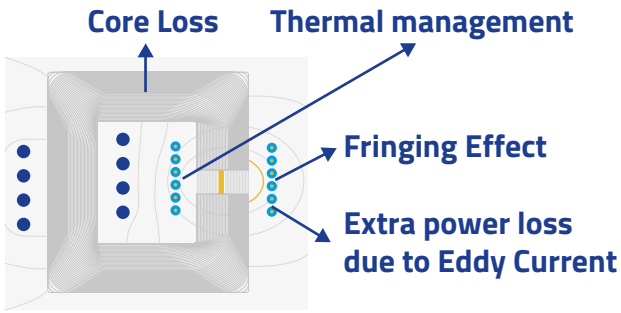
- A greater than 100kV/us Common Mode Transient Immunity (CMTI)
- A propagation delay of less than 50nS and a channel mismatch time of less than 10nS
- An active Miller clamp, which prevents the induced turn-on phenomenon that can occur when another transistor switches. This effect is due to the capacitance of the CGD and the high dv/dt of the switching
- Enough driving capability so that switching can occur at the desired speeds
- A high VIORM (maximum repetitive peak voltage that the isolator can withstand) with the desired maximum working insulation voltage for the final application when high voltage reinforced isolation is necessary. This isolation is also important for high-side applications in many topologies

Some technologies require negative gate voltages, so bipolar sources are necessary. Layout design should also be done meticulously with the aim to:

- Minimize the loop of gate drive
- Minimize the loop of active Miller clamp
- Use a separate gate source, avoiding the introduction of parasitic inductance from the power source loop
- Position the driver components as close as possible to the MOSFET

The use of new magnetic materials is key when introducing SiC transistors in the design of switched converters, which also introduces design challenges such as:

- A higher power density, where the converter-s´switching frequencies must be increased
- An increase in efficiency, where it will be necessary to reduce losses both in the magnetic core and in the wires
- The increase in the switching frequency in the wires, meaning that the skin and the proximity effects are much more critical in the design of the inductive components. This makes it necessary to use litz wires by sets of isolated wires with a smaller section or the use of planar transformers
- In the cores, switching frequency increase leads to an increase in the losses in the materials used for magnetic cores. Also, in the areas with gap the Fringing effect is greater



The use of new materials with a higher temperature range and lower losses has been necessary in materials like:

- PowerCores: used for PFC coils, inverters and resonant chokes
- Ferrites: used mainly for transformers. Among which, for example, the 3C97 material stands out with lower losses, a greater frequency range of use and a greater range of working temperatures

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At PREMIUM we have accepted the challenges this new technology involves and we offer all our Know-how in the design of products at the cutting edge of SiC technology.

Premium is one of the largest power supply companies in Europe, offering solutions to the industrial market being some of them in high-tech machinery, transportation, energy or extreme environments applications. Founded in 1981, Premium designs and manufactures power conversion systems for customers all around the world.

Premium´s power range includes DC/DC converters, uninterrupted power supplies, DC/AC inverters, AC/DC power supplies and any solution that requires high reliability from 50W to 50kW.

Custom is Premium´s standard, so any current product variation or new development can be done by our R&D department, a team of over50 engineers with a wide know-how.

All products comply with the specifications and regulations that each application requires and all projects, from the concept, design anduntil the homologation of the product, are carried out in Barcelona under strict quality controls.

For more information, contact:

Premium Power Supplies
www.premiumpsu.com
hello@premiumpsu.com
+34 932 232 685